

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	3	(james with william with kretchmer)	US-PGPUB; USPAT	OR	ON	2007/06/07 17:12
L3	0	(james with william with kretchmer)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/07 17:12
L4	339	(general adj electric) and (optically near3 active)	US-PGPUB; USPAT	OR	ON	2007/06/07 17:13
L5	5	4 and (SiC or GaN)	US-PGPUB; USPAT	OR	ON	2007/06/07 17:13
L6	2	5 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2007/06/07 17:16
L7	68	((trench or opening or hole or via or aperture or groove) and (SiC or GaN) and oxide and optical\$3).clm.	US-PGPUB; USPAT	OR	ON	2007/06/07 17:22
L8	38	7 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2007/06/07 17:23
L9	11078	((trench or opening or hole or via or aperture or groove) and (SiC or GaN) and oxide and optical\$3)	US-PGPUB; USPAT	OR	ON	2007/06/07 17:23
L10	1577	(trench or opening or hole or via or aperture or groove) and (SiC or GaN) and oxide and (optical\$3 with active)	US-PGPUB; USPAT	OR	ON	2007/06/07 17:26
L11	1052	10 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2007/06/07 17:48
L12	1038	11 not 8	US-PGPUB; USPAT	OR	ON	2007/06/07 17:26
L13	277	12 and (oxide with (trench or opening or hole or via or aperture or groove))	US-PGPUB; USPAT	OR	ON	2007/06/07 17:47
L14	978	438/24,48,218,294,400,429.ccls. and (oxide with (trench or opening or hole or via or aperture or groove))	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49
L15	722	14 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49
L17	113	15 and optical\$3	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49
L18	110	17 not 13	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49

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L19	755	257/510.ccls. and (oxide with (trench or opening or hole or via or aperture or groove))	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49
L20	578	19 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49
L21	40	20 and optical\$3	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49
L22	40	21 not 13	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49
L23	38	22 not 18	US-PGPUB; USPAT	OR	ON	2007/06/07 17:49

DOCUMENT-IDENTIFIER: US 20050040316 A1

TITLE: Vertically integrated photosensor for CMOS imagers

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Application Filing Date - APD (1):

**20030813**

Claims Text - CLTX (2):

1. A method for making an electronic imaging component, said method comprising the steps of: providing an electronics layer; providing a photosensing element, said photosensing element fabricated in a vertically integrated **optically** active layer; providing a substantially vertical interconnect; providing a junction substantially surrounding and at least partially encompassing said vertical interconnect, wherein charge carriers may be substantially laterally drawn toward the axis of at least one of said junction and said interconnect; bonding said **optically** active layer to said electronics layer, wherein said **optically** active layer is disposed substantially proximate to a metalization surface of said electronics layer.

Claims Text - CLTX (5):

4. The method of claim 1, wherein said **optically** active layer comprises at least one of Si, GaAs, InP, **GaN**, HgCdTe, a-Si, p-Si, x-Si, Ge, SiGe, **SiC**, a monocrystalline material, a polycrystalline material and an amorphous material.

Claims Text - CLTX (7):

6. The method of claim 1, wherein said interconnect comprises at least one of a metallized **via**, an electrical conductor, p-Si and a semiconductor; and said interconnect extends substantially through said **optically** active layer.

Claims Text - CLTX (8):

7. A method for making an electronic imaging component array, said method comprising the steps of: providing an electronics array layer; providing a photosensing element array, said photosensing element array fabricated in a vertically integrated **optically** active layer; providing a plurality of substantially vertical interconnects; providing a plurality of junctions substantially surrounding and at least partially encompassing said plurality of vertical interconnects, wherein charge carriers may be substantially laterally drawn toward the axes of at least one of said plurality of junctions and said

plurality of interconnects; bonding said optically active layer to said electronics layer, wherein said optically active layer is disposed substantially proximate to a metalization surface of said electronics layer.

Claims Text - CLTX (10):

9. The method of claim 7, wherein said plurality of interconnects comprise a plurality of at least one of metallized vias, electrical conductors, p-Si and semiconductors.

Claims Text - CLTX (15):

14. The method of claim 7, further comprising the step of providing a plurality of vertically integrated optically active layers.

Claims Text - CLTX (17):

16. The method of claim 7, wherein said optically active layer comprises at least one of Si, GaAs, InP, GaN, HgCdTe, a-Si, p-Si, x-Si, Ge, SiGe, SiC, a monocrystalline material, a polycrystalline material, and an amorphous material.

Claims Text - CLTX (18):

17. A method for making a vertically integrated electronic imaging component, said method comprising the steps of: providing a donor SOI wafer; providing a host CMOS wafer; growing at least one of an intrinsic or p.sup.--epitaxial layer on said donor wafer; growing a thermal oxide layer over said at least one of an intrinsic or p.sup.--epitaxial layer of said donor wafer; optionally forming alignment keys in a Si layer of said donor wafer; said alignment keys corresponding to base keys on said host wafer; defining an optically active, photosensor region in said donor wafer; fabricating at least one photodiode in said donor wafer using a plurality of ion implant steps, wherein charge carriers may be substantially laterally drawn to the axes of junctions formed thereby; optionally forming an optically reflective structure over the top surface of said donor wafer; at least one of planarizing and preparing said donor wafer for bonding; at least one of planarizing and preparing said host wafer for bonding; aligning said host wafer with said donor wafer; bonding said host wafer with said donor wafer through an interface substantially proximate to metal interconnects of said host CMOS wafer; removing substrate material from said donor surface of the resulting donor/host composite structure; etching at least one via within at least one pixel from the donor/host composite structure's top surface down to landing pads of said CMOS wafer; at least one of clearing, metallizing and plugging said vias with a plated metal; optionally re-planarizing the top surface of said donor/host composite structure; optionally forming at least one of a top

side anti-reflecting layer and a top side passivation layer; and **opening** access **vias** to I/O pads embedded in said CMOS wafer.

Claims Text - CLTX (19):

18. The method of claim 17, wherein said **optically** active photosensor region comprises at least one of Si, GaAs, InP, **GaN**, HgCdTe, a-Si, p-Si, x-Si, Ge, SiGe and **SiC**.